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Sheet Lof 2

PTO-1449 (Modified)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

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SERIAL NUMBER 09/492,982

APPLICANT(S)

FARMWALD ET AL.

ORMATION DISCLOSURE STATEMENT
BY APPLICANT

FILING DATE JANUARY 27, 2000 GROUP ART UNIT 2818

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MINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
725	4,330,852	May 18, 1982	Redwine et al.	365	221	
1	4,703,418	Oct. 27, 1987	James	364	200	
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7.55	4,870,562	Sept. 26, 1989	Kimoto et al.	364	200	

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72	, , , _	S56-82961	July 7, 1981	Japan			YES
	1 -	S57-14922	Jan. 26, 1982	Japan			YES
	-	Sho 60-80193	May 8, 1983	Japan			YES
		⁷ Sho 60-55459	Mar. 30, 1985	Japan	·		YES
	_	S61-72350	April 14, 1986	Japan			YES
	1	- S63-142445	June 14, 1988	Japan		_	YES
	_	В63-46864	Sept. 19, 1988	Japan			YES
70	4	S64-29951	Jan. 31, 1989	Japan			YES

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725	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)	
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EXAMINER TANT. NOVEN DATE CONSIDERED 07/31/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.





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TNT.	0 246 767	April 28, 1987	EPO	<u> </u>		
TNT	0 334 552	Mar. 16, 1989	EPO			
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TNIT	European Search Report for EPO Patent Application No. 89 30 2613
TNT	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
TNT	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
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